



VARIABLE GAIN LOW NOISE AMPLIFIER

TECHNICAL FIELD

[0001] The present invention relates to ^gLow Noise Amplifier (hereinafter ~~called~~ ^{referred to as an} "LNA"), more specifically, it is related to a variable gain LNA that is operated most suitably in input matching, gain and noise characteristics, ~~and~~ linearity, etc.

BACKGROUND OF THE INVENTION

[0002] A first terminal is comprised ~~of~~ ^{of} an amplifier that generally amplifies small signal ^s to large signal ^s in wireless equipments, for example a portable phone, TV, etc. This amplifier is ~~demanded~~ ^{made} to have an amplifying operation having

characteristics ~~of~~ low noise and high gain ^{when} the signal is very small. But linearity is demanded rather than the amplifying operation when the signal is relatively large. Therefore, the amplifier satisfies amplifying mode ^s of more than two kinds ^{of} according to input signal level, and it is necessary that the amplifier ^{the} ~~should be selected~~ ^{one of them} in the wireless frequency receiving equipments.

[0003] As a low noise amplifier ⁱⁿ the prior arts, it is disclosed in U.S. Pat. No 6,144,254 that it is possible to switching ^{between} ~~both~~ a low gain and high gain state.

[0004] Fig. 1 shows a circuit diagram of a low noise amplifier disclosed in U. S. Patent No 6,144,254.

[0005] As shown in Fig. 1, the low noise amplifier comprises a common-emitter BN1 (the first NPN transistor to operate in a high gain state), common-base BN2

(the second NPN transistor to operate in a low gain state), third NPN transistor BN3 (the third NPN transistor for provide bias current in BN2) and resistor R1.

[0006] That is, a collector of the first NPN transistor BN1 is connected to an output terminal Pout of ^{an} LNA, a base is connected to an input terminal Pin of ^{an} LNA and the first bias input terminal Bias1, and an emitter is grounded. The resistor R1 is connected between the first bias input terminal Bias1 and first NPN transistor BN1.

[0007] A collector of the second NPN transistor BN2 is connected to the output terminal Pout of LNA, a base is connected to the second bias input terminal Bias2, and an emitter is connected to the input terminal Pin of LNA and a collector of the third NPN transistor BN3.

[0008] A base of BN3 is connected to Bias^{Bias 3}3 (the third bias input terminal), and an emitter is grounded.

[0009] Hereinafter ~~describes~~ ^{the of} an operation of ^{it's described} LNA in the prior arts referring to Fig. 1.

[0010] In the high gain state, Bias^{the}1 is high, and Bias^{the}2 and Bias^{the}3 are low.

Therefore, ^{the first NPN transistor} BN1 is activated and performs the amplifying operation of a high gain, in the high state. Here, ^{the second NPN transistor} BN^{no space}2 and BN^{no space}3 are turned off.

[0011] In the low gain state, Bias^{the}2 and Bias^{the}3 are high, and Bias^{the}1 is low.

Therefore, BN2 and BN3 are activated and perform the amplifying operation of ^{low gain} low gain in the low gain state. Here, BN^{no space}1 is turned off.

[0012] The low noise amplifier shown in Fig. 1 selects one of states between ^{the}

high gain and low gain, and then operates the high-gain or low-gain amplifying

operation in accordance with ^{the} size of the received signal. But, the circuits
operated ^{for} ~~to~~ each gain state ^{are} ~~is~~ affect ^{the} ~~to~~ a load ^{of the} with each other, because input
terminals of the emitter-common first NPN transistor BN1 and base-common

second NPN transistor BN2 are directly connected ^{to} ~~with~~ each other, that is the
base of BN1 is directly connected ^{to} ~~with~~ a emitter of BN2, in the low noise

amplifier shown in Fig. 1. Namely, when the low noise amplifier operates in

^a high gain state, the capacitance of emitter terminal of BN 2 acts as a load ^{an} ~~of~~ ^{no space} ~~for~~

high gain circuits. As a result ~~of that~~, the gain, matching, and ~~the~~ noise

characteristic ^{the} of high gain state are not good, and the capability of the low noise
amplifier is reduced. In addition, when ^{the} low noise amplifier operates in ^{the} low gain

state, the capability of ^{the} low gain state is reduced by the capacitance of the base
terminal of BN1 ^{way as} ~~in the same~~ with high gain state. Because two mode

impedance level of ^{the} input terminal are substantial ^{at} ~~same level~~, ^{by the} ~~and~~ the impedances
^{against} act as a load ~~with~~ each other.

SUMMARY OF THE INVENTION

[0013] The object of the present invention is to provide a variable gain low noise
amplifier ^{in which} ~~that~~ the circuits designed to operate in the best suited ^{way such that} ~~in~~ each gain
mode ^{does} ~~is~~ not affected ^{are} the capability of the best suited to operate in the other
gain mode. ^{circuit}

[0014] Another object of the present invention is to provide ^a variable gain low
noise amplifier ^{for which} ~~that~~ input matching, gain, noise characteristics, linearity, etc can

~~be displayed~~ the capability of the best suited ^{circuit} in ~~each other~~ different mode.^s

[0015] ^{Another} ~~The other~~ object of the present invention is to provide ^a variable gain low noise amplifier which is operated according to the size of receiving signal in more than two amplifying mode^s, and can be varied ^{between} the gain in low gain mode.^s

[0016] ^{Another} ~~The other~~ object of the present invention is to provide variable gain low noise amplifier ^{whose} ~~that~~ power consumption is low.

[0017] ^T ~~According to~~ achieve above objects, a variable gain low noise amplifier, which amplifies the signal applied in an input terminal and outputs to an output terminal, comprises ^{two} ~~a~~ first amplifying cell, which comprises a first terminal and ^{input} second terminal connected to the output terminal, amplifies the signal applied to the first terminal to high gain, and outputs to the second terminal in high gain mode; a second amplifying cell ^{that} ~~comprises~~ ^{that} a first terminal and second terminal connected to the output terminal, amplifies the signal applied to the first terminal to low gain, and outputs to the second terminal in ^a low gain mode; a selectively matching circuit ^{that} ~~comprises~~ a first terminal connected to the input terminal and second terminal connected to the first terminal of the first amplifying cell, and selectively changes an input impedance of the first amplifying cell; a first short-circuit means connected between the input terminal and the first terminal of the amplifying cell, and transmits the signal applied to the input terminal to the first terminal of the second amplifying cell in the operation of low gain mode; and wherein the selectively matching circuit ^{such} ~~changes~~ the input impedance ^{that} the power transmitted to the first amplifying

cell of the signal applied to the input terminal is to be maximum ^{ized} in the operation of high gain mode, and to be minimum ^{ized} of essentially zero in the operation of low gain mode. _{the}

[0018] The variable gain low noise amplifier of the present invention ~~is~~ further comprises a short-circuit means connected between the second terminal of the second amplifying cell and the output terminal.

[0019] The variable gain low noise amplifier of the present invention ~~is~~ further comprises a short-circuit means connected between the input terminal and the output terminal.

[0020] The variable gain low noise amplifier of the present invention, ^{is provided} wherein the first amplifying cell comprises first, second, third terminals, amplifying element, ^{no space} resistor, and ^{degeneration} degradation impedance, and wherein the amplifying element, ^{no space} resistor, and ^{degeneration} degradation impedance ~~are~~ ^{that} controlled the amounts of current ~~flowed~~ from the first terminal to the second terminal in proportion to the voltage applied to the third terminal; and a first terminal of the amplifying element is formed ^{connect to} to the second terminal of the first amplifying cell, the second terminal is connected with one of terminals of the ^{degeneration} degradation impedance, the third terminal is connected with one of terminals of the resistor and then formed ^{connect to} to the first terminal of the first amplifying cell, the other terminal of the resistor is applied to the HG-bias voltage of activating the first amplifying cell in an operation of high gain mode, the other terminal of the ^{degeneration} degradation impedance is grounded, and the amplifying element is connected to common mode of the

second terminal.

[0021] The variable gain low noise amplifier of the present invention, ^{is provided} wherein the second amplifying cell comprises a first, second, and third terminals; a first amplifying element controlled ^{by} the amounts of current flowed ^{ing} from the first terminal to the second terminal in proportion to the voltage applied to the third terminal; wherein the second terminal of the first amplifying element is formed ^{connect to} to the first terminal of the second amplifying cell, and the third terminal is applied to the LG-bias voltage ^{to} of activating ^e the second amplifying cell in the ^{the} operation of low gain mode, and the first amplifying element comprises an amplifying unit connected to ^a common mode of the third terminal; and ^{the} second and third amplifying element, ^{that} voltage source, and variable voltage source, ^{the} which are controlled ^{that} the amounts of current flowed from the first terminal to the second terminal in proportion to the voltage applied to the third terminal; wherein the first terminal of the second amplifying element is formed to the second terminal of the second amplifying cell, the second terminal is connected to the first terminal of the first amplifying element of the amplifying unit by connecting with the second terminal of the third amplifying element, the third terminal is connected ^{to} with one of the terminals of the voltage source, the first terminal of the third amplifying element is connected to the power source, the third terminal is connected to the variable voltage source, and the other terminals of the voltage source and variable voltage source are grounded. ^{is provided}

[0022] A variable gain low noise amplifier of the present invention, wherein the

matching circuit comprises a first and second inductor, capacitor, and short-circuit means; and one of the terminals of the first inductor is connected with the second inductor and the capacitor, the other terminal is connected to the short-circuit means, the other terminal of the second inductor is formed ^{of the} first terminal of the matching circuit, the other terminal of the capacitor is formed to ^{connect to} ~~the~~ ^{the} second terminal of the matching circuit, and the other terminal of the short-circuit means is grounded.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Fig. 1 shows a circuit diagram of a low noise amplifier ^{of} ~~in~~ the prior arts.

[0024] Fig. 2a shows a circuit diagram of a source-common amplifier ^{of} ~~in~~ the prior arts.

[0025] Fig. 2b shows a circuit diagram of a gate-common amplifier ^{of} ~~in~~ the prior arts.

[0026] Fig. 3 shows a circuit diagram of a variable gain LNA according to an embodiment of the present invention.

[0027] Fig. 4 shows a circuit diagram of a variable gain LNA according to another embodiment of the present invention.

[0028] Fig. 5a shows a circuit diagram of a first amplifying cell according to ~~an~~ ^{for} ~~embodiment of~~ the present invention ^{as} the variable gain LNA showed ⁿ ~~ed~~ in Fig. 3 ^{or} ~~and~~ Fig. 4.

[0029] Fig. 5b shows a circuit diagram of a second amplifying cell according to ~~an embodiment of~~ the present invention ^{for} ~~as~~ the variable gain LNA showed ⁿ ~~ed~~ in Fig.

3^{or} and Fig. 4.

[0030] Fig. 5c shows a circuit diagram of a selectively matching circuit according to an embodiment of the present invention ^{for} as the variable gain LNA shown in Fig. 3^{or} and Fig. 4.

[0031] Fig. 6a shows a circuit diagram of the variable gain low noise amplifier shown in Fig. 3 using circuits shown in Fig 5a, 5b and 5c.

[0032] Fig. 6b shows an equivalent circuit diagram of ^{an} the input part of the first amplifying cell in order to describe the operation of selective matching circuit^s in accordance with an embodiment of the present invention, when the variable gain low noise amplifier is operated in high gain mode.

[0033] Fig. 6c shows an equivalent circuit diagram of the input part of the first amplifying cell in order to describe the operation of selective matching circuit in accordance with an embodiment of the present invention, when the variable gain low noise amplifier is operated in ^{low} low gain mode.

DETAILED DESCRIPTION

[0034] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the attached drawings.

[0035] Here, a common source and gate low noise amplifier ^{the} of prior arts will be described, and then proper embodiments of a variable gain low noise amplifier according to present invention will be described in detail with reference to the attached drawings.

[0036] Fig 2a shows a common source amplifier ^{of the} in prior arts.

^(Referring to)
 [0037] ^a ~~Showing in~~ Fig. 2, a common source amplifier comprises ^{an} NMOS transistor MS21, first inductor L21, second inductor L22 and third inductor L23, resistor R21 and voltage source V21. The drain of ^{the} NMOS transistor MS21 is formed to ^{connect to} an output terminal Pout connected with one of terminals of first inductor L21, the gate is connected with ^{the} resistor R21 and third inductor L23, and the source is connected with one of ^{the} terminals of ^{the} second inductor L22. The other terminal of ^{the} first inductor L21 is connected to a power source VDD, and the other terminal of ^{the} second inductor L22 is grounded, and the other terminal of third inductor L23 is formed to ^{connect to} an input terminal Pin of the amplifier. The voltage source V21 is connected between the other terminal of the resistor R21 and ^{the} ground.

[0038] The common source amplifier showed ^{n in} Fig. 2a amplifies the signal applied through the input terminal Pin to ^{in a} high gain ^{mode}, and can be matched ^{to} the input power and noise through a ^{degeneration} ~~degradation~~ ^{the} of source. Accordingly, the source common amplifier is proper to ^{ize} get a maximum noise characteristic and gain. But, it ^{is} ~~is a~~ weak point that linearity is bad due to a voltage amplification effect ~~of~~ caused by capacitance of ^{the} third inductor L23 and NMOS transistor MS21.

[0039] Fig. 2b shows circuit diagram of gate common amplifier ^{of the} ~~in~~ prior arts.

[0040] ⁿ ~~Showed~~ in Fig. 2b, the gate common amplifier comprises a NMOS transistor MG21, an inductor L24, a capacitor C21 and a current source I21. The drain of the NMOS transistor MG21 is formed to ^{connect to} an output terminal Pout of the amplifier connected with one of the terminals of the inductor L24, the gate

is connected to one of the terminals of the voltage source V22, and the source is connected ^{to} with one of the terminals of the current source I21 and capacitor C21. The other terminal of the voltage source V22 is grounded, the other terminal of the inductor L24 is connected to the power VDD and the other terminal of the current source I21 is grounded. The other terminal of the capacitor C21 is formed ^{connect to} to an input terminal Pin of the amplifier.

[0041] The gate common amplifier showed ⁿ in Fig. 2b amplifies the signal applied through the input terminal Pin ^{in a mode} to low gain. Because it cannot ~~be get an~~ effect ^{for in} of voltage amplification ~~to use an~~ input matching circuit in the gate common amplifier, the gain and noise characteristic ^{are} is bad ~~to compare~~ with the source common amplifier showed ⁿ in Fig. 2a. But, it is easy to match an input resistance through the gm value by controlling of ^{the that s to} current flowed in the

transistor ~~(NMOS)~~ because the input resistance is $1/g_m$. The value of the input resistance is much smaller than that of the source common amplifier showed ⁿ in Fig. 2a. It ^{is} a strong point ^{obtain} that the gate common amplifier can ~~get~~ a very high linearity ^{compared to} more than the source common amplifier, because the linearity of gm is superior in case ^{s in which} of a recently developed transistor ^{has a} having small channel length.

And it is easy for the gate common amplifier to operate a variable gain function by means of addition ^{in a} of the circuit ~~which is~~ to vary the output current in the output terminal of the amplifier.

[0042] Hereinafter ~~describes~~ an embodiment of a variable gain low noise amplifier (LNA). ^{is described}

[0043] The variable gain LNA according to the present invention makes ~~the~~ use of an amplification element that is a MOSFET transistor. The amplification element comprises a gate, source and drain. The MOSFET transistor has the characteristics that ~~amounts to~~ ^{allow} the direction of a current ~~flowed~~ ^{to be} from the source to the drain or the other way ~~is~~ decided according to the value and polarity of the voltage applied to the gate. Other amplification elements like the MOSFET are a bipolar junction transistor (BJT), junction field effect transistor (JFET), metal oxide semiconductor field effect transistor (MOSFET), metal semiconductor field effect transistor (MESFET), etc.

[0044] Hereinafter describes mostly the MOSFET among the above amplification elements. But the spirit and scope of the present invention is not limited to the MOSFET element and may be applied all the other equivalent elements. And hereinafter describes mostly an N type MOSFET, but it is obvious to those skilled in the arts that the spirit and scope of the present invention may be applied to a P type MOSFET ^{and is} not limited to the N type MOSFET.

[0045] Fig. 3 shows a circuit diagram of a variable gain LNA according to an embodiment of the present invention.

^{As} [0046] ~~Showed~~ ⁿ in Fig. 3, the variable gain LNA according to an embodiment of the present invention comprises a first amplifying cell 3100, second amplifying cell 3300, selectively matching circuit 3500, and first means of short circuit ^{or switch} SW1. The first amplifying cell 3100 comprises a first terminal 301 and second terminal 303, and amplifies a signal applied to the first terminal 301 ^{for} ~~to~~ high gain

white ing as minimize an additional noise^{the} in high gain mode. The second amplifying cell

3300 comprises a first terminal 305 and second terminal 307, and amplifies a signal applied to the first terminal 305 ^{to} as control the gain^{the} in low gain mode.

The selectively matching circuit 3500 comprises a first and second terminal 309, 311 and selectively changes an input impedance of the first amplifying cell 3100 for that the circuit operated in each gain mode does not act on a load respectively.

[0047] Hereinafter describes the connection^s relation of these, referring to Fig. 3. ^{the LNA of} ^{are} ~~described~~

[0048] The first terminal 301 of the first amplifying cell 3100 is connected ^{to} with the second terminal 311 of the selectively matching circuit 3500, and the

second terminal 303 is connected ^{to} with the second terminal 307 of the second amplifying cell 3300 and formed ^{connect to} to an output terminal Pout of LNA. ^{the} The first

terminal 305 of the second amplifying cell 3300 is connected ^{to} with the first short-circuit means ^{or switch} SW1. The first terminal 309 of the selectively matching

circuit 3500 is connected ^{to} with the other terminal of the first short-circuit means ^{or switch} SW1 and formed ^{connect to} to an input terminal Pin of LNA. ^{the}

[0049] ^{As} ~~Shown~~ in Fig. 3, the third short-circuit terminal may ^{be} comprised between the second terminal 307 of the second amplifying cell 3300 and the output ^{set}

terminal Pout in the variable gain LNA according to an embodiment of the present invention. And that, ^{with the structure} the output signal of the second amplifying cell

3300 outputs to the output terminal of the LNA due to the third short-circuit means ^{or switch} SW3 in the ^{operation} of the low gain mode.

[0050] Hereinafter ~~describes~~ an operation of the variable gain LNA according to an embodiment of the present invention. *will be described*

[0051] The variable gain LNA ~~is~~ operated ^{as} in two ~~mode~~^s, ~~that is~~ ^a high gain ^{mode} and low gain ~~mode~~^s according to ^{the} a power level of a received signal. That is, it ~~is~~ operated ^s in high gain mode when the power level of the received signal is under ^{the} a threshold power decided beforehand, and operated ^s in low gain mode when ^a the power level of the received signal ~~is over~~ ^{exceeds} the threshold power. *that has been*

[0052] The short-circuit means may reduce the signal due to having a ~~disregardless~~ resistance value in the state of short-circuit, and may ~~be~~ operated ^{with} a load ~~due to~~ ^{that can be disregarded} having a finiteness reactance value in the ~~state of~~ open-circuit, when it is operated ^{the} in high gain mode. Accordingly, ~~it must restrain to~~ ^{be used} use the short-circuit means in the circuit operated in high gain mode, and the above load characteristics of the short-circuit means must be carefully considered ^{for} in case of each amplification circuit operation ^{and} respectively.

[0053] When ^{when} it is high gain mode, the first amplification cell 3100 is activated ^{by that} the first short-circuit means SW1 is opened and HG-bias is applied to the first amplifying cell 3100. And the second amplifying cell 3300 is inert by ^{not} ~~non-~~ applying LG-bias. *an*

[0054] Accordingly, when it is operated ^{the} in high gain mode, the impedance of the second amplifying cell ~~3500~~ ³³⁰⁰ operated in low gain mode ^{the} ~~is~~ ^{does} not ^a effect to the first amplifying cell 3100 operated in high gain mode by ^{the} opening of the first short-circuit means SW1, and only the open impedance of the first short-circuit means

affects
~~is effect to~~ the high gain mode circuit. But, the input of the first amplifying cell 3100 operated in high gain mode is generally matched to 50 ~ 70 ohm, that is standard resistance. ~~Due to~~ the selectively matching circuit 3500, the open impedance of the first short-circuit means SW1 ~~is so~~ ^{has a} high value ^{of} more than 50 ~ 70 ohm. So, the effect ^{of} ~~that~~ the open impedance ^{having} ~~is to~~ a load for the first amplifying cell 3100 is ignored. Accordingly, the variable gain LNA according to an embodiment of the present invention may be the most suitable operation in high gain mode, and amplifies the input signal ^{for a} ~~to~~ high gain.

[0055] When ^{in the} ~~it is~~ low gain mode, the second amplifying cell 3300 is activated by ~~that~~ the first short-circuit means ^{being} ~~is~~ shorted and LG-bias ~~is~~ applied. And, the first amplifying cell 3100 is inert by ^{not} ~~not~~ applying HG-bias. The selectively matching circuit 3500 changes the input impedance of the first amplifying cell 3100 in low gain mode to high impedance ^a ~~more than~~ ^{of} the ^{above mentioned} ~~beforehand~~ decided value (generally standard resistance value: 50 ~ 75 ohm). Accordingly, ^{the} in low gain mode the variable gain LNA may be the most suitable operation because the first amplifying cell 3100 is not operated ^{to bear} ~~to~~ a load of the second amplifying cell 3300 ^{the} in low gain mode.

[0056] Fig. 4 shows a circuit diagram of a variable gain LNA according to another embodiment of the present invention.

[0057] The embodiment showed ⁱⁿ ~~ed~~ in Fig. 4 is different ^{from} ~~to~~ the variable gain LNA according to the embodiment showed ⁱⁿ ~~ed~~ in Fig. 3 in the point that ^a fourth short-circuit means ^{or switch} SW4 is ^{arranged} ~~comprised~~ between the input terminal Pin and output ^{the}

terminal Pout. The variable gain LNA according to another embodiment of the present invention directly transmits the received signal to the output terminal Pout through the fourth short-circuit means. So, power consumption may be reduced according to this embodiment. Moreover high linearity is provided and signal distortion is reduced by eliminating an input signal level of post part (normally mixer) of the variable gain LNA.

[0058] Fig. 5a shows a circuit diagram of a first amplifying cell according to an embodiment of the present invention in the variable gain LNA showedⁱⁿ in Fig. 3 and Fig. 4.

[0059] As shown in Fig. 5a, the first amplifying cell 3100 is embodied in¹⁹ common-source, and comprises an amplifying element MS51, ~~degradation~~^{degeneration} impedance DI51, and resistor R51. The drain of the amplifying element MS51 is formed to^{connect to} the second terminal 303 of the first amplifying cell 3100, the gate is connected to the terminal of the resistor R51 and is formed to^{connect to} the first terminal 301 of the first amplifying cell 3100, and the source is connected to a terminal of ~~degradation~~^{degeneration} impedance DI51. In the other terminal of ~~resistance~~^{the or} R51, when ~~high gain mode operates~~^{operating in the}, the first amplifying cell 3100 is activated by HG-biasing voltage, ~~the other terminal of degradation impedance DI51 is~~^{and} grounded. ~~Degradation~~^{degeneration} impedance DI51 can be ~~embodied~~^{made} to use the passive or the active elements of resistor and inductor, etc.

[0060] As mentioned above, the common-source amplifier has excellent noise and gain characteristics, and can get satisfying input power and noise matching

results
 at the same time, through the ^{degeneration} ~~degradation~~ impedance DI51 connected to the source of the amplifying element MS51. Also, as shown in Fig. 3, the common-source amplifier can ~~be displayed~~ the capability of the best suited ^{circuit for} ~~in~~ ^{the} noise and gain side ^s because ~~the~~ matching circuit 3500 is connected to the first terminal of the first amplifying cell 3100. Therefore, when the low noise amplifier is used ^{with} ~~to~~ the above common-source amplifier in the high gain mode which need ^{sa} high gain amplifying operation, it can ~~be displayed~~ ^{its utmost} ~~the most~~ capability ^{ies}.

[0061] Fig. 5b is a circuit diagram for showing ^{the} inside structure of the second amplifying cell 3300 in accordance with an embodiment of the present invention ~~x~~ in ^{the} variable gain low noise amplifier shown in Fig. 3 ^{or} ~~and~~ Fig. 4.

[0062] As shown in Fig. 5b, the second amplifying cell 3300 is embodied in ^a common-gate, and comprises an amplifying part 510 and gain part 530.

[0063] The amplifying part 510 of the second amplifying cell 3300 comprises the first amplifying element MG51. The drain of the first amplifying element MG51 is connected to the connecting point of the source of the second and third amplifying element MG52, MG53 of ^{the} variable gain part, and when operating ^{in the} low gain mode, LG-biasing voltage ^{that} ~~to be~~ activate ^s the second amplifying cell 3300 is driven, and source is formed ^{the} ~~at~~ the first terminal 305 of the second amplifying cell 3300.

[0064] In ^a variable gain low noise amplifier in accordance with an embodiment of the present invention, preferably, ^{the} current source ~~be~~ ^{please} not shown, refer to Fig. 2)

is provided between the source of the first amplifying element MG51 and ground. In this case, it can be changed trans-conductance (gm) data of the first amplifying element MG51, and it can be controlled input impedance data of the amplifying part 510, by control of current source data.

[0065] A variable gain part 530 comprises the second and the third amplifying elements MG52, MG53 and voltage source V51 and variable voltage source V52. The drain of the second amplifying element MG52 is formed the second terminal 307 of the second amplifying cell 3300, and gate is connected to one of terminal of voltage source V51, source is connected to the third amplifying element MG53. The drain of the third amplifying element MG53 is connected to the power source VDD, gate is connected to variable voltage source V52. The drain of the third amplifying element MG53 is connected to power source VDD, gate is connected to variable voltage source V52.

[0066] An amplifying part 510 comprises the first amplifying element MG51 connected to common-gate, and amplifies the signal driven in the first terminal 305 of the second amplifying cell 3300. As mentioned above, common-gate amplifier can easily controlled input matching, and it has an excellent linearity.

[0067] As the variable gain part 530 controls the current quantities which divided the current came from amplifying part into the second and the third amplifying elements MG52, MG53, by the control of variable voltage source V52, the variable gain part 530 can vary the output came from the second terminal 307 of the second amplifying cell 3300, and it can control in

succession the gain data of the second amplifying cell 3300. In addition,

because the current of the first amplifying element MG51 is not changed by

~~the~~ variable gain part 530, the trans-conductance data of the first amplifying element MG51 is regular, the input matching of the second amplifying cell 3300 is not changed.

[0068] Therefore, if ~~the~~ variable gain part is used ~~in~~ the second amplifying cell 3300, which has common-gate construction shown in Fig. 5b, ~~the~~ in low gain mode, it can perform successive variable gain function^s without changing the characteristic of input matching, and a low noise amplifier can be ~~gotten~~ ^{provided with} an excellent linearity.

[0069] Fig. 5c is a circuit diagram for showing ^a selective matching circuit 3500 in accordance with an embodiment of the present invention, ~~in~~ ^{or the} variable gain low noise amplifier shown in Fig. 3 ^{or} ~~and~~ Fig. 4.

[0070] As shown in Fig. 5c, the selective matching circuit 3500 in accordance with an embodiment of the present invention comprises the first and the second inductor^s L51, L52 and capacitor C51 and the second short circuit-means ^{or switch} SW2.

[0071] One of the terminals of the first inductor L51 is connected to the second inductor L52 and capacitor C51, the other terminal is connected to one of the terminals of the second short circuit-means SW2. The other terminal of the second inductor L52 is formed ^{to connect to} the first terminal 309 of selective matching circuit 3500, the other terminal of capacitor C51 is formed ^{the} the second terminal 311 of ^{to connect to} selective matching circuit 3500, the other terminal of the second short circuit-means SW2 is grounded.

[0072] In the selective matching circuit 3500 in accordance with an embodiment of the present invention, the second short circuit-means SW2 can ~~be~~ displayed the capability of the best suited ^{in which} ~~in the state of~~ the first amplifying cell 3300 is activated ^{by} high gain mode driven HG-biasing; in case of low gain mode, i.e., ~~as~~ ^{to have an} HG-biasing is not driven, the selective matching circuit 3500 is selected ~~the~~ input impedance of the high gain mode circuit block which is made ^{by} selective matching circuit 3500 and the first amplifying cell 3100, in case the first amplifying cell 3100 is not activated.

[0073] Fig. 6a shows a circuit diagram of ^{the} ~~the~~ variable gain low noise amplifier shown in Fig. 3 using circuits shown in Fig 5a, 5b, and 5c.

[0074] As shown in Fig 6a, ^a variable gain low noise amplifier in accordance with an embodiment of the present invention comprises the first and second amplifying cell ^{3100, 3300 and} ~~the~~ selective matching circuit 3500, and the first short circuit-means ^{or switch} ~~SW1~~.

[0075] The first amplifying cell 3100 is embodied in the form of ^a common-source and is operated ⁱⁿ ~~the~~ high gain mode, and the second amplifying cell 3300 is embodied in the form of ^a common-gate and is operated ⁱⁿ ~~the~~ low gain mode. Moreover, ^{the} selective matching circuit 3500 comprises the second short circuit-means, and in high gain mode, the input of the first amplifying cell 3100 is matched ^{by} ~~the~~ selective matching circuit 3500 in order that the first amplifying cell 3100 can ~~be~~ displayed ^{the} the capability of the best suited; ^{and} ~~and~~ in low gain mode, the input impedance of the first amplifying cell 3100 is changed ⁱⁿ ~~in~~ a high data ^{to}

^{mode} by selective matching circuit 3500, and the first amplifying cell 3100 is not ^{the} operated ^{using} as the load of the second amplifying cell 3300. Therefore, ^{the} variable gain low noise amplifier in accordance with an embodiment of the present invention can ~~be displayed~~ ^{circuit} the capability of the best suited in each gain mode.

[0076] Also, ^a variable gain low noise amplifier in accordance with an embodiment of the present invention ~~is used~~ ^{is with a} common-source the first amplifying cell 3100 in ^{the} high gain mode ^{that} demanded high noise and gain characteristic, and ~~is used~~ ^{is} a common-gate ^{with} the second amplifying cell 3100 in low gain mode ^{that} demanded high linearity and successive variable gain, as a consequence of that, ^a linearity is good and input matching is easy, and ^{the} amplifier can ~~be embodied~~ ^{have a} variable gain low noise amplifier ^{with} which is possible successive variable gain function.

[0077] Furthermore, in case the power level of ^{the} receiving signal is enough large and amplifying is not need, ^{ed because the} as receiving signal is directly passed ^{to the} in output terminal by the fourth short circuit-means ^{as switch} SW4 shown in Fig. 4, power consumption ^{that is} demanded for amplifying operation is not need. ^{the} ~~conversion~~ ^{needed}

[0078] Fig. 6b and Fig. 6c are circuit diagrams shown in equivalent ^{the} the input part ^{of} of the first amplifying cell 3100 in order to described more specifically the operation of ^{the} selective matching circuit 3500 in accordance with an embodiment of the present invention, ^{the} in case variable gain low noise amplifier is operated in ^{the} each high gain mode ^{or the} and low gain mode.

[0079] In ^{the} case of high gain mode, the second short circuit-means is open, and the input ~~of~~ ^{is} activated the first amplifying cell 3100 can be shown in a

equivalent ZHG, on. At this time, ^{space} variable gain low noise amplifier can ^{the} be ^{realize} gotten the capability of the best suited ^{circuit} by matching the input impedance of the first amplifying cell 3100 by ~~means of~~ using the second inductor L52 and capacitor C51. That is, because the electric powers of ^{the} variable gain low noise amplifier and the first amplifying cell 3100, the high gain mode characteristic of the best suited ^{circuit realized} can be gotten.

[0080] In ^{the} case of low gain mode, the second short circuit-means is short, and inactivated ^{ins} the input of the first amplifying cell 3100 can be shown in a equivalent ZLG, off. Here, ZLG, off ^{space} is ^{space} as shown in the views is ^{as shown in the views is} very different ^{from the} from the ZHG, on data; ^{the} this time, ^{in case} matching circuit 3500 comprises the first and the second inductor L51, L52 and capacitor C51. The first inductor L51 ^{handles} has the inductance data that the input part of the first amplifying ^{are sent to} cell 3100 ^{providing} seems the substantial infinite input impedance ^{from the} in node 309. As it does ^{the} this way, in case of low gain mode, the input part of the first amplifying cell 3100 is not affected ^{by} in the second amplifying cell 3300. Therefore, the input of ^{the} variable gain low noise amplifier is matched ^{to} in the most ^{suitable of} fitted the input of the second amplifying cell 3300, because the maximum power P_{in} is transferred, ^{and at the same time,} and at the same time, the power of the first amplifying cell 3100 is substantial zero, ^{by thus,} variable gain low noise amplifier ^{realizes} is ^{gotten} the low gain mode characteristic of the best suited ^{circuit}.

INDUSTRIAL APPLICABILITY

[0081] In a low noise amplifier in accordance with the present invention, because the operating circuits in each gain mode is not affected ^{by} in the

performance of the operating circuit of the best suited ^{circuit of} to the other gain mode,
~~the~~ each circuits ~~can be displayed~~ the capability ~~of the best suited~~ ^{to} in the each
mode.

[0082] Also, input matching, gain, noise characteristic and linearity etc, can be
displayed ~~the capability of the best suited~~ ^{to} in the each other ⁱⁿ different gain mode.

[0083] Further, ~~the~~ each circuits ^{s a} is operated ^{with at least} in gain mode more than two
according to the size of receiving signals, and can be varied ^{the} gain in low gain
mode.

[0084] Furthermore, because the output of each circuits ^{can} ~~get to be equal~~ to the
receiving signals by the short circuit-means, ~~in case~~ amplifying operation is not
^{needed} the power consumption is reduced.